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Dynamic shortcut circuits - concept and case study for static scenarios

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Abstract

Introduction of circuits into the packet-switched network influences the QoS of the packets transported hop by hop. This report focuses on the correct dimensioning of two types of circuits in a butterfly network with different loads. The results show that depending on the load and routing mechanism, introduction of circuits can bring benefits for both the packets transported by the circuits and the packets transported by the packet-switched network with reduced resources.

Packet switched networks are very efficient in terms of utilization of network resources, but the service they provide is usually dependent on the traffic conditions. Traffic in the Internet is hardly predictable, and so is the end-to-end transmission delay of packets. Moreover, each hop on a packet route is a potential congestion point and may cause variation of the transmission delay or even packet loss. Usage of a circuit in an IP network guarantees a constant delay and no losses between its edges, namely high and predictable QoS. An investigation of influence of circuits in the packet switched network was performed in this report, with the focus set on circuit dimensioning. It was shown that circuits in the Internet can decrease packet transmission delay and losses, while increasing throughput, if lowly utilized links are used to establish a circuit.

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1 Introduction

Together with the increasing popularity of the Internet, the expectations on the Quality of Service (QoS) it provides have increased. Due to the packet switched nature of the Internet each node adds variable delay to packets traversing the node. This delay is highly dependent on the traffic that flows through the network. Additionally a packet can be lost at each node due to congestion.

One solution to overcome these drawbacks and improve the QoS is to integrate circuit switching - analogical as in the Public Switched Telephone Network - into the Internet. A circuit is a connection with reserved bandwidth between two IP nodes. E.g. a circuit can be provided by an SDH connection which traverses several transit SDH nodes. It reduces the number of IP hops to one and decreases the load at transit IP routers. Packets in a circuit experience small, traffic-independent delay without jitter at the transit SDH nodes, but at the same time a circuit may cause inefficiencies by reducing the bandwidth for the packets outside the circuit due to over-provisioning [14].

The most important questions that need to be answered (mainly due to dynamic nature of traffic) are:

- Between which nodes to establish a circuit?
- How should a circuit be dimensioned?
- Under which conditions (e.g. amount of traffic) should a circuit be established/released?
- What is the influence of a circuit on packets outside the circuit?

Our research aims at answering these questions to increase the QoS by introduction of dynamically established circuits with possibly smallest and negligible over-provisioning. There has been a lot of work done in the field of Routing & Wavelength Assignment (RWA) ([3], also with traffic triggered by load variation [8], [2]), however traffic prediction without global knowledge about the current traffic in the network remains a challenge [7]. Especially dimensioning of circuits has not been tackled so far in the literature. Different criteria can be used to dimension circuits. Although physical network links are underutilized nowadays [11], their capacity is limited. Therefore the capacity of the circuits can be overprovisioned up to a certain limit. The higher the overprovisioning, the smaller the probability of congestion at the beginning of the circuit, and the higher the QoS the packets traversing the circuit experience. If the improvement of QoS is to be prioritized over efficient usage of network ressources, some over-provisioning can be tolerable.

The rest of this report is structured as follows. Network architecture and different kinds of circuits are described in Section 2. Their performance is investigated in Section 3 (two scenarios under variable load). Eventually conclusions are drawn and future work is discussed.

2 Circuits - a way to increase QoS

2.1 Approach

As shown in Fig. 1, network architecture may consist of at least two layers, i.e. the IP layer and the data link/physical layer. The connection between two IP nodes (routers or end-systems) consists of circuits in the lower layer.

We assume that the circuits can be dynamically established and released depending on the available resources (bandwidth) of the physical layer. We assume that the bandwidth of the physical links can be shared among multiple circuits with the granularity of 1 b/s, and that they use all the available bandwidth in the network. Therefore in order to establish a new circuit we have to decrease the bandwidth of some of the old circuits. Access of the new circuits can be restricted to certain classes of packets.

The circuits can be provided with SDH or other technologies like WDM, ATM, OTH or IP Switching [9, 12]. Newer solutions which offer circuits are ORION (Overspill Routing In Optical Network) [4], APSON (Adaptive Path Switched Optical Network) [13] and CHEETAH (circuit-switched high-speed end-to-end transport architecture) [15, 17]. In some sense MPLS and GMPLS [6] or TCP Switching [10] provide possibilities to dynamically establish circuits. A circuit in each technology grooms packets that use the circuit. Some policies determining when to establish circuits have been discussed in [7] (Flow Switching). In addition, we address the question how to dimension and layout a circuit. The dimensioning of a circuit should increase QoS in the circuit. At the same time over-provisioning and overhead related to the setup of the circuits should be kept small in order not to decrease QoS of packets, which are not allowed to use the circuits. Another reason to establish a circuit is the avoidance of congestion in the IP network - a circuit is a way to bypass congested IP nodes. Motivation for establishing circuits is not restricted to the reasons above. No matter what the reason, a dimensioning of the

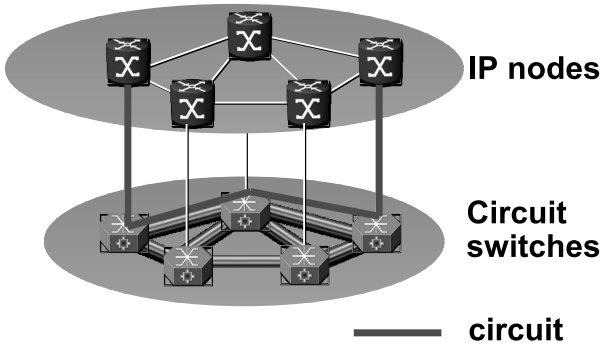

Figure 1: Network architecture - IP network on the top of a circuit switched layer

circuits is needed.

In all cases we lay out a circuit via least utilized links to achieve a homogeneous load distribution in the network (load balancing). This means that the circuit does not need to go via the shortest path.

The circuits are theoretically not restricted to routers - any pair of end-systems can be connected by a circuit. A full meshed network is not feasible though due to limited network capacity and scalability reasons (addressing of each link). Circuits can only be established between routers at the edges of the backbone (edge-routers) in our approach. We call circuits that connect edge-routers end-to-end circuits. The end-to-end circuits are used to increase the QoS of a single flow (originated at the node, where the circuit begins, and destined to the node, where circuit terminates). We define a flow as a sequence of all packets originated at one edge router and destined to another one. If the circuit is used to bypass congested nodes, so that the circuit connects transit-routers and not necessarily edge-routers, we call it a by-pass circuit. The by-pass circuit can be used by multiple flows. Over-provisioning of by-pass circuits is expected to be lower compared to end-to-end circuits, because traffic of a single flow between edge-routers is more bursty than aggregated traffic in the network. In contrast to end-to-end circuits, multiple flows can benefit from a by-pass circuit, however improvement of QoS per flow is expected to be lower.

2.2 Metrics

The following metrics are used to measure QoS in the networks with and without circuits:

- Packet loss rate - amount of packets in a flow that are lost in respect to the total amount of packets in the network
- Transmission delay - time between the moment of packet generation and the moment of its arrival at the destination
- Transmission jitter - difference between transmission delays of subsequent packets

Performance of the network is measured with the following metrics:

- Throughput - amount of bytes that have left the network in a given period of time
- Network utilization - average percentage of network resources (links' bandwidths) in use
- Link utilization - average percentage of link bandwidth in use
- Packet drops - amount of packets dropped a) at certain nodes; b) in certain flows; c) in the whole network

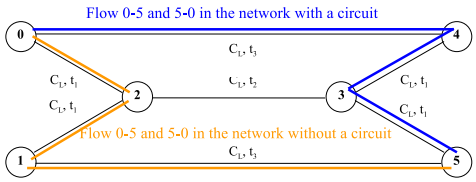

Figure 2: Scenario 1

3 Simulation experiments

Investigation of potential of QoS improvement vs. over-provisioning for end-to-end and by-pass circuits compared to a pure packet switched network was performed with simulation experiments. The results of simulation of the pure packet switched network without any circuits serve as a reference for results of simulation of networks with circuits. We choose network scenarios, which are simple to follow the influences of multiple network parameters on its performance and the QoS.

Simulation experiments under different traffic and load conditions were performed to answer the following questions:

- How does establishment of an end-to-end or by-pass circuit influence flows outside the new circuit?
- How should these circuits be dimensioned in Dependance from the load?
- At which load level does establishment of a circuit pay off?

We use ”X->Y” to denote a flow or unidirectional circuit from node X to node Y, and ”X<->Y” to denote a bidirectional circuit between nodes X and Y.

3.1 Scenarios

3.1.1 Scenario 1: End-to-end circuit with load balancing

A circuit reserves bandwidth on a link, reducing the available bandwidth for the old links of the IP layer. Such a reduction may create bottlenecks. Scenario 1, shown in Fig. 2, is primarily used to investigate the influence of an end-to-end circuit on the

Table 1: Link utilization - reference network (2.0 Gbps per traffic generator)

Link	0->2	0->4	1->2	1->5	2->3	3->4	3->5
Utilization [%]	99.35	52.58	99.35	52.58	52.28	39.33	39.36
Link	2->0	4->0	2->1	5->1	3->2	4->3	5->3
Utilization [%]	99.35	59.04	99.35	59.04	59.21	39.33	39.33

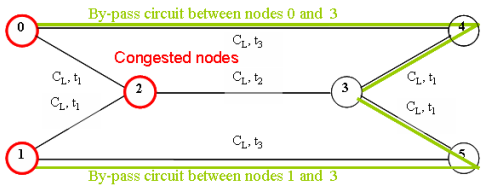

Figure 3: Scenario 2

Table 2: Percentage of packets dropped out of all packets dropped - network without circuits

Node	0	1	2	3	4	5
Load 1.6 Gbps/Flow	0	0	0	0	0	0
Load 2.0 Gbps/Flow	33.47	33.37	33.16	0	0	0
Load 2.4 Gbps/Flow	33.43	33.44	33.13	0	0	0

packets outside the circuit. The reference IP topology is identical as the physical topology.

Flows 0->5 and 5->0 were selected to be transported via the new circuit, as they traverse the biggest amount of hops in the IP network[1]. They are transported via nodes 0, 2, 1 and 5 in the reference network (routes calculated with the Dijkstra algorithm [14], where all the links have equal weights, and no ECMP is used). Two bottleneck links have been determined by a prior investigation of the reference scenario: between nodes 0 and 2 and nodes 1 and 2 - see Table 1.

Multiple paths offer multiple choices to lay out a circuit. The alternative paths are used to balance the load (to reduce the number of congested nodes). For simplicity reasons scenario 1 restricts the number of alternative paths to two, namely 0, 4, 3, 5 and 0, 2, 3, 5. The a prior investigation has shown that the utilization of links on the first path is lower (see Table 1). Therefore it has been selected for the circuit.

3.1.2 Scenario 2: By-pass circuits with load balancing

Simulation of the reference packet-switched network has shown that losses occur at nodes 0, 1, and 2 (at the inputs to bidirectional links 0<->2 and 1<->2) - see Table 2. Therefore we investigate by-pass circuits to reduce congestion. We establish a bidirectional by-pass circuit between nodes 0 and 3 (Fig. 3) to bypass nodes 0 and 2. A second by-pass circuit is established between nodes 1 and 3 to bypass nodes 1 and 2. Flows 0->5 and 0->3 and contrariwise use circuit 0<->3, and the Flows 1->5 and 1->3 and contrariwise use circuit 1<->3.

[1]Flows 1->4 and 4->1 could also be chosen for investigation, as they are symmetric to Flows 0->5 and 5->0

3.2 Simulation parameters

All simulations have been performed by ns-2 with the Circuit Switching Module developed in TKN, TU Berlin. All links have capacity C_L = 9.95328 Gbps, corresponding to the STM-64 data stream (with overhead). Traffic is generated according to Poisson Model. Average bit rate (constant for every simulation) is varied from 1.6 to 2.4 Gbps with a step of 0.2 Gbps (not all results are presented in this report), and is equal for every flow (each node generates packets to every other node). Packets have constant size of 1500 Bytes. Buffer size is set to 5706 packets [1, 5, 16]. Propagation delays are set to t_1=0.87 ms, t_2=1.60 ms and t_3=2.74 ms. The circuit capacity C_{CS} and load were varied.

Since zero IP processing delay has been assumed so far in all scenarios, packet end-to-end delay consists only of the queuing delay, transmission delay and propagation delay. Each bypassed IP router causes additional saving on an end-to-end delay of a packet. The results of simulation experiments are discussed in the following section. All the plots shown there present dependence of various metrics on capacity of a circuit C_{CS} and traffic generated by a traffic source (corresponding to a flow). The capacity of a circuit is given as percentage of link capacity (STM-64).

3.3 Results

The results show that for packets traversing a new circuit the expected reduction (in comparison to reference network) of the transmission delay can indeed be achieved (Figures 4, 5 and Table 3) depending on the load. Regarding the average transmission delay of all packets in the network (Figures 6 and 7), a reduction can only be achieved if the load does not exceed a certain threshold value. If the network load is above the threshold value, the network operates in a saturated or overloaded state, and the benefits of the multiplexing gain in pure packet switched networks with big links outperform the benefits of new circuits. Even that the transmission delay increases for highly loaded networks, the loss rate decreases and the throughput increases independently from the load (see Figures 10 and 12). The results of simulations show that jitter in the considered scenarios is so small that it can be neglected.

We discuss the results in details in the following sections.

3.3.1 Influence of new circuits on QoS

Establishment of a circuit can improve QoS not only for packets traversing the circuit, but also for the rest of the packets. The packet loss rate is smaller than in the reference network for all loads and can even be eliminated in both packets using and not using new circuits (Figures 8, 9 and Table 3). This is due to the layout of the circuit over lowly underutilized links, which leads to better distribution of load over the network.

Regarding end-to-end transmission delay (Figures 4 and 5), circuits in the considered Scenarios have no influence on PSPN at low load (1.6 Gbps per flow), if

circuit capacity is $\sim 50\%$ of the link capacity (in both Scenarios). If circuit capacity is too small, transmission delay of the CSPN increases - there is insufficient bandwidth reserved for packets that are to be sent via the circuit, so they have to traverse a highly filled buffer which shapes bursty traffic at the edge of the circuit.

The higher the load, the higher link capacity needs to be reserved for the circuit to avoid increase of transmission delay in CSPN (or even packet losses). Similarly to the previously discussed case, increasing the circuit capacity results in an increase of transmission delay in the PSPN. If the load is too high, the link has insufficient capacity for both PSPN and CSPN resulting also in an increased transmission delay. The increase of transmission delay in PSPN can be recognized at the same circuit capacity value independent from the circuit type (end-to-end or by-pass circuits), namely at circuit capacity equal to 28% of link capacity for load 2.4 Gbps per flow, 40% for load equal to 2.0 Gbps per flow, and 50% for load 1.6 Gbps per flow (see Figures 4 and 5). Choosing circuit capacity above these values means prioritization of packets in the new circuits over other packets (degradation of QoS they experience).

3.3.2 Choice of the circuit capacity

The circuit is well dimensioned if QoS in the circuit is improved without degradation of QoS of any packets, meaning that all considered metrics (packet loss rate, transmission delay and network throughput) over the whole network are optimized. All three parameters can be improved only if the network is not overloaded. As discussed in the previous section, in order to avoid degradation of QoS of packets not using new circuits, the circuit capacity shall not exceed a load dependent threshold. A discussion of the minimum required circuit capacity follows below. The difference between minimum circuit capacity and maximum allowed circuit capacity is denoted as circuit tolerance.

Tolerance of end-to-end circuits to improper dimensioning is higher than in by-pass circuits. Figures 8 and 9 show that the range of circuit capacity, where the losses are eliminated, is broader in Scenario 1 (end-to-end circuit) than in Scenario 2 (by-pass circuits). At the load 2.0 Gbps per flow, this range for end-to-end circuit spans from 20 to 40% of the link capacity. In the case of by-pass circuits (no matter if one or two of them are used) it can actually take just a value of 40% of the link capacity (the by-pass circuit carries two flows and not one, therefore it needs to have higher capacity). The higher the load, the smaller the range where packet losses are eliminated. This fact is confirmed by behavior of transmission delay (Figures 6 and 7). Moreover, at circuit capacity equal to 40% of the link capacity, the minimum transmission delay changes to a maximum for higher loads (see curves for 2.0 and 2.4 Gbps per flow in Fig. 7). The maximum results from insufficient capacity for all packets (inside and outside the circuit). Increasing the circuit capacity above 40% of the link capacity decreases transmission delay of the packets using circuits. This also decreases the overall delay. Decreasing the circuit capacity below 40% of the link capacity increases the available capacity of old circuits, and also leads to

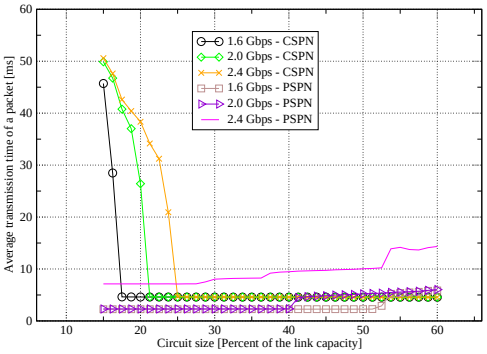

Figure 4: Transmission time of packets in CSPN and PSPN at different loads - scenario 1 (CSPN denotes all flows that use circuits, PSPN denotes flows that use no circuits. This applies also to the following figures)

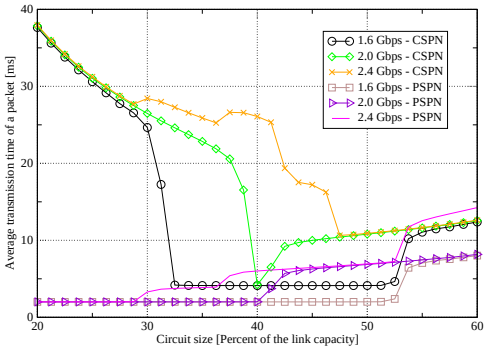

Figure 5: Transmission time of packets in CSPN and PSPN at different loads - scenario 2 (CSPN denotes all flows that use new circuits, PSPN denotes flows that use no circuits. This applies also to the following figures)

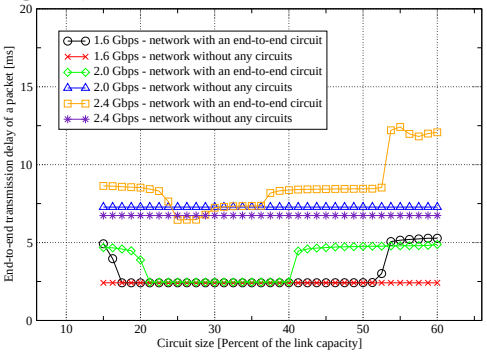

Figure 6: Average transmission time at different loads - scenario 1

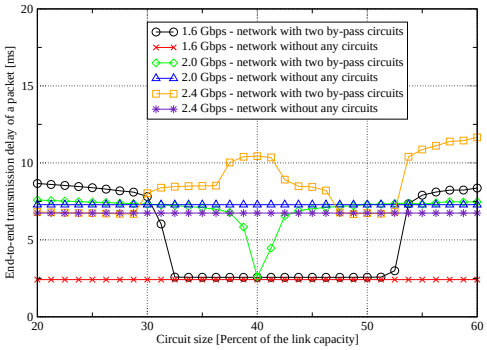

Figure 7: Average transmission time at different loads - scenario 2

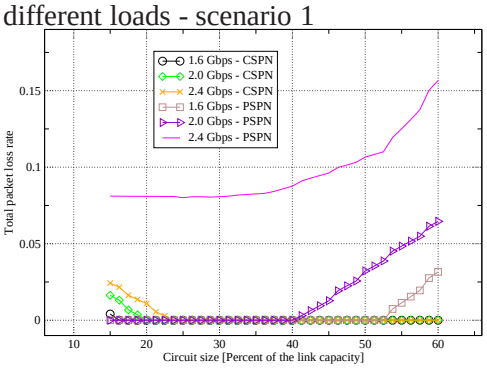

Figure 8: Packet loss rate at different loads - scenario 1

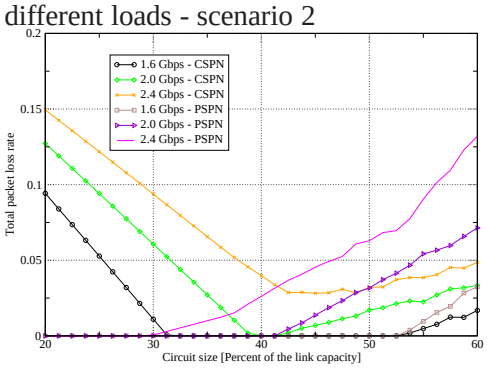

Figure 9: Packet loss rate at different loads - scenario 2

Table 3: Packet loss rate and transmission delay - network without circuits

	Scenario 1			
Load	PLR of SF	PLR of OF	TD of SF	TD of OF
1.6 Gbps/Flow	0	0	4.570	2.264
2.0 Gbps/Flow	0.016	0.078	18.133	7.115
2.4 Gbps/Flow	0.029	0.147	18.263	7.161
	Scenario 2			
Load	PLR of SF	PLR of OF	TD of SF	TD of OF
1.6 Gbps/Flow	0	0	3.556	2.003
2.0 Gbps/Flow	0.044	0.045	13.682	5.687
2.4 Gbps/Flow	0.085	0.087	13.748	5.713

PLR = packet loss rate; TD = transmission delay im ms; SF = Selected Flows = Flows that use a new circuit; OF = Other Flows, not SF
SF for Scenario 1: 0->5, 5->0
SF for Scenario 2: 0->5, 5->0, 0->3, 3->0, 1->4, 4->1, 1->3, 3->1

a decreased delay of packets disallowed to use new circuits, and the overall delay. This corresponds to increased packet losses though (Fig. 9).

Figures 10 and 12 presenting network throughput show that the circuit capacity should be set to 30% of the link capacity (for Scenario 1) and 40% of the link capacity (for Scenario 2) in order to maximize throughput. The lower the load, the bigger the tolerance of circuit dimensioning regarding network throughput.

Network throughput can be increased in comparison to a network without circuits under all considered traffic loads (Figures 10 and 12). Moreover, when using by-pass circuits, an increase of network throughput (denoted as $ratio\_Thrpt\_i$) results in a proportionally lower increase of network utilization $ratio\_U\_i$ (the network utilization even decreases in scenario 2 - see Fig. 13). The increase of utilization in a network with an end-to-end circuit is proportional to the increase of network throughput (see Figures 10 and 11). This is due to the better usage of resources reserved by a circuit in case of a by-pass circuit (the circuit is used by more then one flow, so the over-provisioning of the circuit is smaller here due to multiplexing gain).

It can be observed in Fig. 9 (Scenario 2 with two by-pass circuits) that the packet drops of packets using new circuits occur when the circuits is both under- and overdimensioned. The first case is quite intuitive - the reason of losses is a deficit of bandwidth in the underdimensioned circuits. The packet losses in the second case occur due to the fact that establishment of new circuits leads to a lower capacity of the old circuits in the network. This causes losses of packets leaving the new circuits and entering the old ones (of reduced capacity). E.g. Flow 0->5

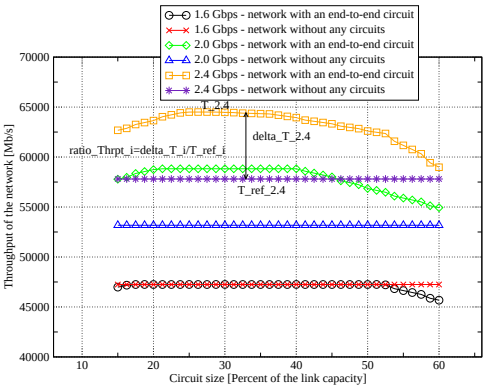

Figure 10: Network throughput at different loads - scenario 1

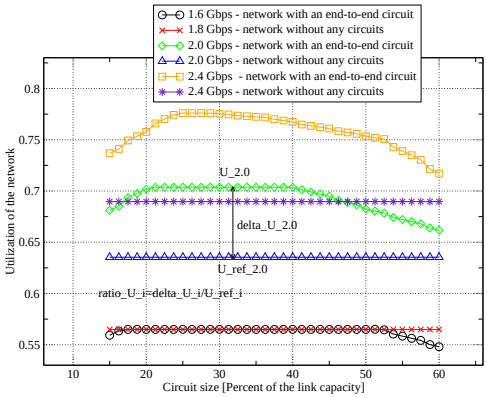

Figure 11: Network utilization at different loads - scenario 1

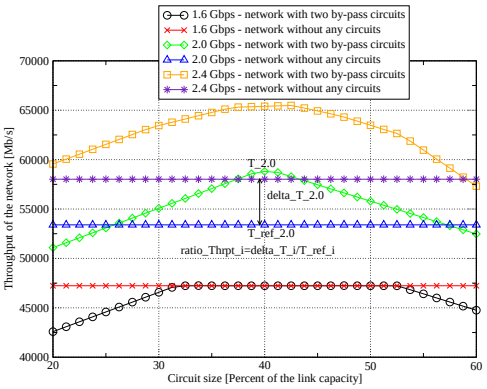

Figure 12: Network throughput at different loads - scenario 2

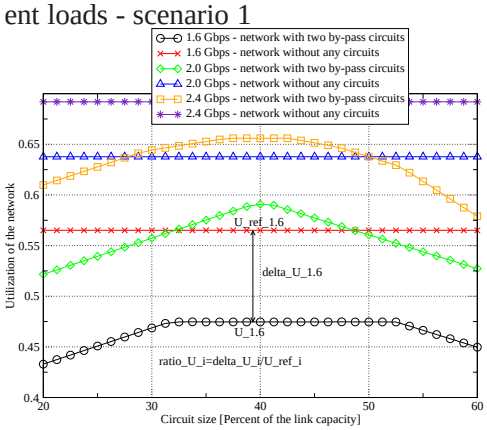

Figure 13: Network utilization at different loads - scenario 2

(Fig. 3) is transported by a circuit up to node 3, and then it uses the resources of a link between node 3 and node 5. If the capacity at link 3->5 is too small (due to the overdimensioned circuit 3->1), then the packet loss rate increases.

4 Summary and future work

This report presented performance of end-to-end and by-pass circuits in two network scenarios. Establishment of a circuit can improve QoS of packets using this circuit and also of other packets, depending on the load and the chosen circuit capacity. It was also found out that end-to-end circuits are significantly easier to dimension than the by-pass circuits. Changes of size of an end-to-end circuit under medium load have little influence on the QoS. Similar changes of size of a by-pass circuit can lead to a dramatic decrease of QoS. The by-pass circuits are more scalable than end-to-end circuits (important especially in bigger networks). Moreover,

as a by-pass circuit is used by more than one flow, the multiplexing gain inside the circuit provides lower network utilization than using end-to-end circuits (assuming the same network throughput). Increase of throughput in a network with by-pass circuits can even be accompanied by decrease of network utilization!

In order to confirm the conclusions drawn above, bigger networks need to be investigated. The bigger the network, the more possibilities to lay out a circuit. So far we considered traffic model without the closed loop relationship, which in connection-oriented traffic like TCP may have significant impact on the performance of our concept. Therefore TCP traffic needs to be considered too. Independent from the kind of traffic, an architecture, where packets overloading the new circuits are redirected into the old ones, can be investigated. This approach reduces losses of the packets using circuits, but may cause reordering of packets. In addition, more realistic models (like measurement based traffic characterization and the introduction of IP processing time) are expected to confirm the obtained results.

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