Xilinx FPGA design using Simulink with Hardware Co-Simulation

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Outline

1. Introduction
2. Design toolchain
3. Basic Elements
4. Demo - FFT calculation
5. Summary
Simulink based FPGA design model

**Simulink**

Environment for multidomain simulation and Model-Based Design for dynamic and embedded systems.

**Xilinx System Generator**

High-level tool for designing high-performance DSP systems using FPGAs.

- Replace HDL language with Simulink blocks
- Xilinx Blockset contains many functions
- Possibility to use HDL modules as black boxes
- Ease of simulation and testbench
- Compilation to bitstream, HDL, hardware co-simulation
Hardware co-simulation

Incorporate hardware into Simulink design

- Speed up simulation with hardware in the loop
- Automatic data exchange
- Supports Xilinx FPGA chips with JTAG programming
Required software

- Matlab
- Matlab Simulink
- ISE Design Suite
- EDK
- System Generator
- Additional software: Mentor Modelsim
Toolchain

Required software

**The MathWorks**
- Matlab 7.4.0.287 (R2007a)
- Matlab Simulink 6.6 (R2007a)

**XILINX**
- ISE Design Suite v10.1.03
- EDK v10.1.03
- System Generator 10.1.3.1386

- Sensitive to version changes
- One System Generator supports only two Matlab versions
- Xilinx ISE v10.1 is the last one supporting Virtex II chips
- Additional software: Mentor Modelsim
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Simple example

- System Generator
- Input/Output Gateway
- Xilinx blocks
- Any Simulink blocks

- Gateways are Top-level output in compilation results
- Between gateways there are only Xilinx blocks
- Outside gateways can be all other blocks
System Generator

- Most important block
- Must be at Top-level in every Simulink model
- Allows compilation of the design
System Generator compilation targets

- HDL Netlist
  - VHDL
  - Verilog
- Bitstream
- Hardware co-simulation
  - JTAG
    - FPGA programming
    - Data exchange
- Ethernet
  - Data exchange
  - Point-to-point
  - Network based
Gateways

- Name is transferred to the generated IP
- Fixed binary point arithmetic
- Important to set Output data type
  - number of bits
  - binary point
Basic elements

System Generator
Addressable Shift Register
Assert
BitBasher
Black Box
Clock Enable Probe
Concat
Constant
Convert
Counter
Delay
Down Sample
Expression
Gateway In
Gateway Out
Memory library

- Addressable Shift Register
- Delay
- Dual Port RAM
- ROM
- Register
- Shared Memory
- Single Port RAM
- FIFO
- LFSR
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Simulink model

- Signal generated in Simulink. Sum of 2 sine waves and noise
- 512point FFT
- Delay block on *done* line
Hardware-Software Co-Simulation

- Simulink subsystem with Xilinx blocks
- Compiled Co-Simulation block
  - Automatic JTAG connection
  - FPGA configuration at simulation start
Demo results

Calculated FFT

Done, synchronization pulse

Original signal
Summary

Simulink as FPGA design tool
- Easy to use
- No need of HDL knowledge
- Multiple ready blocks

Hardware-Software Co-Simulation
Xilinx System Generator brings hardware into simulation

Problems
- Sensitive to version changes
- Complicated and long toolchain
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